Electromagnetic compatibility (EMC) in several gate charging topologies for Automotive Power Switches

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***Abstract*— this paper presents several charge - discharge blocks for gate driver circuit of a high side automotive power switch. A comparison of these topologies regarding electromagnetic emissions is achieved.**

I. INDRODUCTION

In nowadays automotive circuitry an important role is played by the power switch. This is used to drive different types of loads, from bulbs to leds. This paper is focused on a new technique to charge the gate of a high side power switch for a good EMC behavior. Three different command circuits are analyzed and simulated in order to estimate the low frequency electromagnetic emissions.

II. HIGH SIDE SWITCH IN AUTOMOTIVE

The power switch is present in the automotive environment to drive different loads as led, bulbs or motors.

The most common power switch is the double diffused MOS (DMOS) transistor, for the advantages that it offers compared to bipolar transistor [1-6].

A vertical structure is used because it can sustain large voltages and high currents. Its disadvantage is that all the DMOS devices on a wafer have a common drain. In auto motive applications this is not a problem because transistor drains are always connected to the battery [1-3].

As the switching topology we use the high side configuration. The advantages are that the high side power switch is a 1 wire system; the short to ground cannot destroy load and load corrosion is unlikely. A high side switch is a device which is connected between the battery line and load. The main disadvantages are that it is less robust, with distributed ground and it has a more complex design, meaning it is more expensive. [1-3]

Electromagnetic compatibility (EMC) has become very important in the last years due to the more and more electronics in a car and the continuous shrinking of the devices. EMC can be defined as “the ability of an electronic system to function properly in its intended electromagnetic environment, and to not contribute interference to other systems in the environment.”[5].

The pulse width modulation (PWM) mode, when the switch is turned on and off with a certain frequency, is generally an emission source. In the low frequency spectre will appear harmonics of the switching frequency. To diminish these harmonics, which cause emissions, we need to reduce current slew rate. Due to power losses the slew rate cannot decrease too much. Hence a trade-off between loss of power and emissions is desired.

The charging/discharging current of the power switch gate is, typical, constant in automotive applications [1]. A high current, used to drive the switch gate in order to minimize power losses, determines sudden variations on the output characteristics of the switch, as shown in *Fig. 1*. The sharp corners that can be observed on the output curve from *Fig.1* are responsible to large emissions. The power losses are influenced by the increase/ decrease slope of the output voltage, only. Small currents correspond to the output voltage time diagrams corners and a larger current is preferred for the transition period. Based on this observation we propose to charge the switch gate by three methods, using different currents.

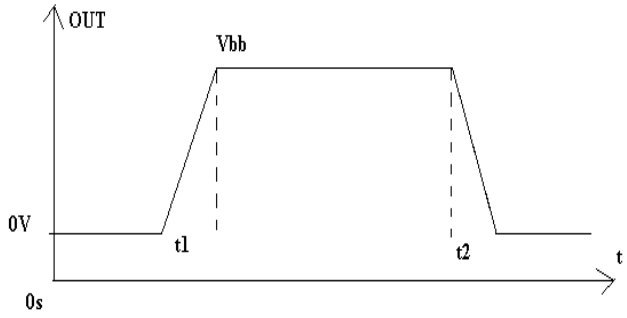

Fig. 1 Turn on and off transition

Turning on and off the switch produces interferences with a wide frequency spectrum, that are generated by the internal circuitry. The use of Fourier transformations enables these signal forms, which are periodic in time, to be analyzed in the frequency domain. From the fundamental frequency of the signal up to the first corner frequency fg1, the graph of the spectrum is parallel to the frequency axis. After the first corner frequency, the amplitude reduces by 20dB/decade up to the second corner frequency fg2, from where the spectrum falls off by 40dB/decade [2].

The first pole, fg1, is given by the PWM switching frequency, whiles the second pole, fg2 is given by the turn on/off times. If we have a longer turn on/off time (smaller

slew rate) the second pole moves to the left. In case we have edge shaping the decreasing rate after the second pole is increasing, meaning that we will have smaller emissions.

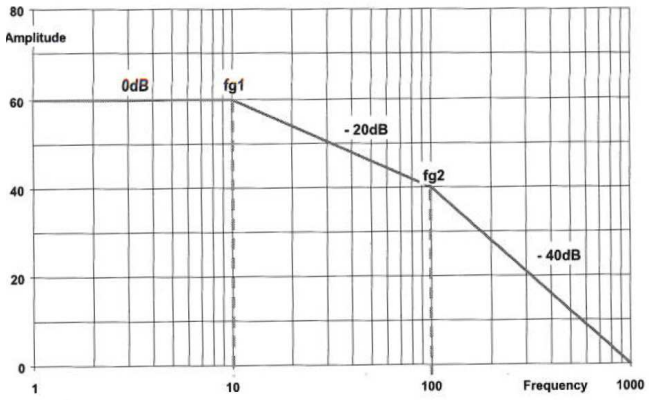

Fig. 2 Frequency spectrum

III. GATE DRIVER PRINCIPLE

The power switch device needs a driver circuit in order to turn it on and off and to keep it in the safe operating area. A concept schematic of this circuit is presented in *Fig. 3* [1].

The charge pump block was figured to show that the driver circuit is supplied between the charge pump voltages VCP and OUT.

The *turn off block* is driven by the enable channel command which will discharge the gate with a constant current. We also have a fast discharge in case of over temperature. The *turn on block* is sinking current from the charge pump and is sourcing a constant current to the gate of the power device.

The *current limiting block* is reading a sense voltage on a sense resistor and if this increases over a certain level it generates the over current (OC) signal.

The *overvoltage block* is referring to the difference between battery and OUT. If this is higher than a certain level the power switch device will be turned on to reduce the voltage across it so that the device will not be destroyed..

The *clamping block* is referring to EMC. In case the switch is off the gate of the power device is strong connected to the output, its source, so that the circuit will be immune to the emissions of other circuits.

In this paper we will focus only on the *charge/discharge block*, to see how different topologies of gate charging currents influence the emissions in PWM mode.

Three different topologies will be implemented and compared. The first one will be the simplest when the gate is charged with constant current.

The second topology will charge the gate with a small current until a certain threshold and after that will step the charging current to o larger value to ensure the slew rate parameter.

The third topology will be an improvement of the second one, because the charging current will not just be stepped, but will increase linearly to the slew rate value, this giving us lower emissions.

A. Constant current topology

As already stated this topology uses a constant current to charge the gate of the power transistor. A concept schematic is presented in *Fig. 4*.

The I_SR_bias current that will be mirrored out with an m factor, by the current mirror MP1:MP3. MP2 transistor is giving the current for the discharge path.

When we have ON command we close the switch SW1 and let the I_SR_bias current multiplied by *m* charge the gate of the double diffused power transistor (MD).

Receiving an OFF command will open SW_1 and close SW_2 so that the MD gate will be discharged by the NMOS transistor (MN2).

I_SR_bias is such chosen in order to assure the slew rate of the device (here comes the name SR).

The constant current is chose to ensure the slew rate of the power switch.

B. Stepped current topology

This topology in an improvement of the constant current one, because we charge the gate with a small current, so we will have more rounded edges, and after the voltage (or the current) at the output raises we will commute to the large current. The large current is chose so that to ensure the slew rate and the small current so that to ensure lower emissions.

A concept schematic is presented in *Fig 5*. We need a comparator to detect when the output voltage (current) becomes large enough so that to switch the gate charging current to the high value.

In this topology we use a current (I_Small_Current) to decrease the current from I_SR_bias in order to have a reduced charging current when the output voltage (current) is small.

When we detect that a certain output voltage (current) level have been reached we open the switch SW_3 and let all I_SR_bias current to be mirrored out to charge the gate of the power transistor.

The additional circuitry is not too much area consuming due the fact that we only need another mirror for the small current (I_Small_Current) and a comparator to detect the level at the output, voltage or current.

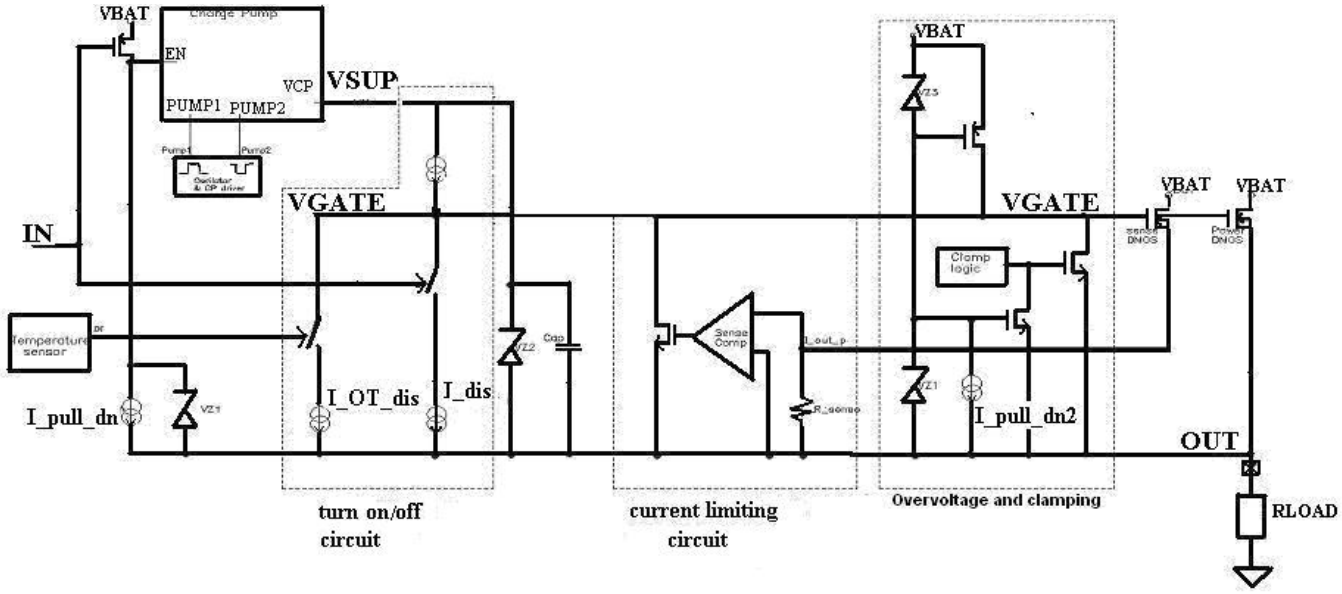

Fig. 3 Driver circuit

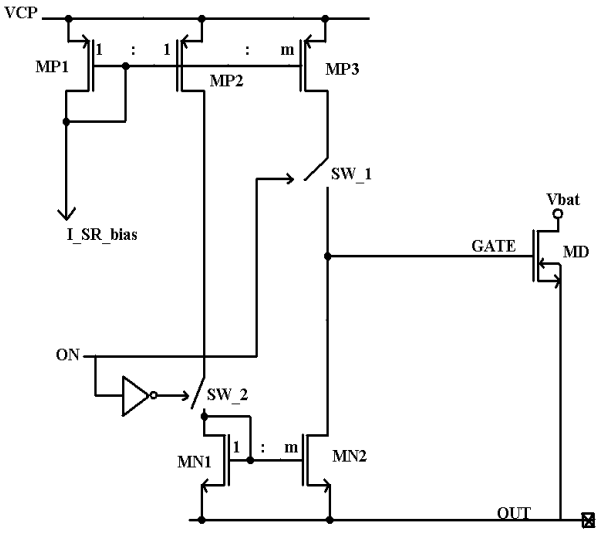

Fig. 4. Constant current topology

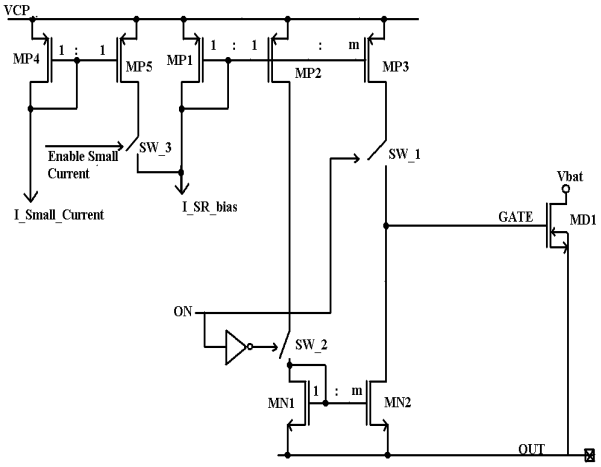

Fig. 5. Stepped current topology

C. Linear current topology

This topology is improving the stepped current one by linearly increasing the small current to the slew rate current, in order not to have a large variation in the charging currents.

A concept schematic is presented in *Fig. 6*. For this topology we need an additional circuitry that will increase the charging current linearly to the output voltage (current).

In this topology we do not use SW_3 from topology B, but we design I_pull current in order to be large when the output voltage (current) is small and to linearly decrease to zero when the output voltage (current) is reaching a certain threshold. This means that when output is low (under the threshold, I_pull 90% of I_SR_bias and only a small current is mirrored out to charge the gate of the power device. This

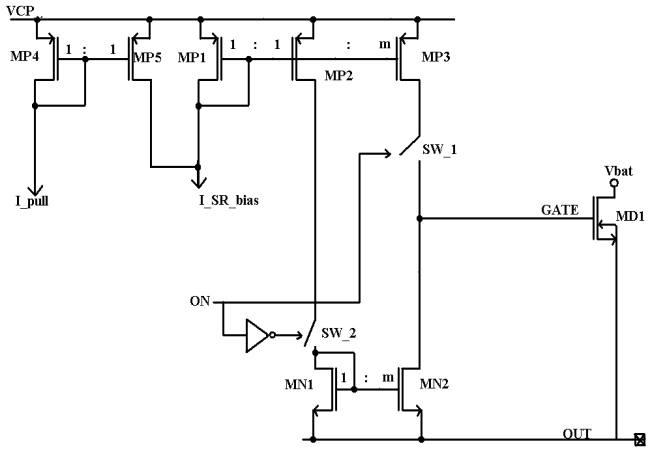

Fig. 6. Linear current topology

means that we will round the lower corner of the output characteristic.

The additional circuitry is a bit larger that the topology B because we need now I_pull to be proportional to the output voltage (current) and to be 0 when the threshold has been reached. But, with a good design the area increase was insignificant considering to the EMC improvement.

IV. EMC COMPARISON FOR THE THREE TOPOLOGIES

In order to compare the three topologies we will simulate the circuit in the same configurations. The device under test (DUT) is the turn on/off block from one of the three topologies. In order to simulate the real life behavior we will introduce the DUT in the gate driver schematic and run a full chip simulation, for a 20mOhm power switch device. The comparison will be discussed for conducted emissions only.

The emissions requirements are as follows. In the 150kHz to 300kHz the amplitude of the interferences should be smaller than 72dBuV. In the range of 500kHz to 2 MHz the emission should not exceed 64dBuV.

The simulation setup is presented in Fig. 7. We connect the full chip to the supply through a LISN (Line Impedance Stabilization Network) in order to simulate the real life connection to the battery, where we have a parasitic inductance of the connection wire and parasitic capacitance to ground. The readings of the emissions are done at net "meas" terminal. For the result we will Fourier transform the time domain wave at "meas" in order to obtain the frequency domain wave, the spectrum.

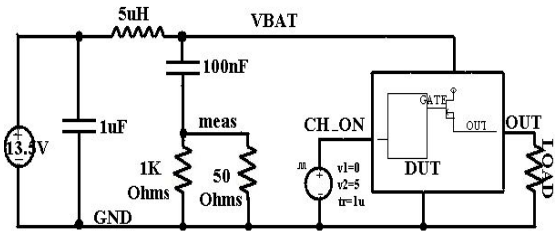

Fig. 7. LISN electromagnetic emissions simulation setup

The comparison is done after the low frequency emissions because this is the band where it is the improvement of the edge shaping technique. In the high frequency domain the most important emitting block is the charge pump.

For a better view on the differences we plot the emissions for the three topologies on the same graph, which you may find in Fig. 8. Here, on the x axis we have the frequency in MHz, and on the y axis the amplitude of the emissions in dBuV. The x axis scale is linear, expressed in MHz, for an easier reading of the emissions.

As we can see the worst emissions spectrum has the first topology with no additional edge shaping circuitry.

The second topology has better emissions but at the limit of 72dBuV in 150KHz – 300 KHz. Taking into account that this is just a simulation we should have some margin so that we will not reach the limit when we will have process variation.

The third topology has only 50dBuV emissions in the low frequency domain, which is a very good result, giving us more than 20dBuV margin until the limit of 72dBuV is reached that is giving us confident that the silicon will also fulfill the requirements.

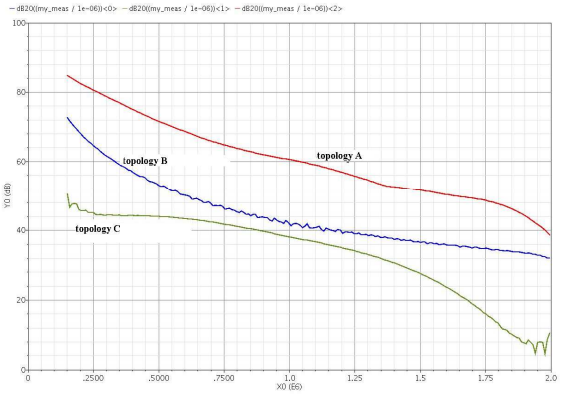

Fig. 8. LISN electromagnetic emissions simulation results

V. CONCLUSIONS

We have presented three different topologies to drive the gate of the double diffused power MOS transistor. We discussed the concepts schematic differences and presented a comparison regarding the conducted emissions.

The first topology is charging the gate of the switch with a constant current and has no edge shaping circuitry, giving us the worst emissions.

The second topology is based on 2 charging currents, one small at the lower corner of the characteristic and one larger in the slew rate region. This topology has better emissions, but at the limit giving us no margin with process variation.

The third topology is based on linearly increasing the charging current. It has the best emissions, having a comfortable margin of 20dBuV.

VI. REFERENCES

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